Group Members:  
________________________________________________________________________________
________________________________________________________________________________
________________________________________________________________________________

**Grading of Lab Demonstration**
Board should be setup at start of demo. Programmer is connected to board. Quartus is open, set up, and ready to program the board. The Verilog design used at demo must be the same design that was submitted as a text file with the lab report. MIDI-OX should be open and ready to play.

| Press reset button on board, play note on keyboard, play second note on keyboard after releasing first note | /5  |
| LEDS turn on when first note played | /5  |
| Note number shown on LEDs matches the note shown in MIDI-OX | /5  |
| LEDS remain lit until key is released, at which point they turn off until next note | /10 |
| Second note played works correctly, and shows the new note number | /5  |

**Examine and discuss Verilog code**
- Verilog design uses more than one module | /5  |
- No combinational logic (other than reset) included within “always @(posedge clk)” block | /5  |

**Lab Demonstration Total**  
/35

**Grading of Lab Report**

| Report describes contribution of each group member | /5  |
| Part 1: (see pg3 of lab description for details) | |
| Number of registers and latches given before and after removing the default case | /5  |
| Explanation of why removing default case changes the results | /5  |

**Part 2:**

**Quartus Simulation Waveforms:**
- Simulation waveforms show at least 2 full MIDI bytes arriving on input | /3 |
- LEDs shown as simulation outputs, and values change appropriately on second byte | /4 |
- Value of MIDI note number and the corresponding LED value annotated in text on waveforms | /4 |
- Analysis of whether simulation is correct and how you reached this conclusion | /4 |

**Logic Analyzer Printouts:**
- Single printout shows MIDI signal and LEDs turning on and off (MIDI values need not be readable) | /5 |
- Printout annotated with text of note number shown on the LEDs (don’t annotate MIDI input) | /5 |
- Analysis of whether printout shows correct behavior and how you reached this conclusion | /5 |

**Explanation of Design:**
- Hierarchy of modules explained clearly | /3 |
- Schematic diagrams from RTL viewer, using specified Quartus settings, for each module | /3 |
- Table listing all registers in the design | /4 |

**Part 3:**
- Correct analysis of maximum tolerable clock frequency | /10 |

**Lab Report Total**  
/65

**Deductions**

| Submitted with wrong group: 30pt deduction if lab 4 group members are different from lab 2 group members and the change was not approved in an email | |
| Lateness: Assignment is complete when all three files are submitted: report/code/self-assessment. 20pt deduction for 1 day late. No submissions accepted more than 1 day late due to end of semester. | |

**Overall Lab Score**  
/100